BCM43526

5G WiFi IEEE 802.11ac Draft 2×2 Dual-Band Single-Chip Solution

GENERAL DESCRIPTION

The BCM43526 is a dual-band (2.4 GHz and 5 GHz) 5G WiFi 2 × 2 compliant MAC/PHY/Radio complete System-on-a-Chip. This 5G WiFi device enables the development of USB WLAN client and media solutions that can take advantage of the extremely high throughput and extended range of the Broadcom® 5G WiFi solution. With 5G WiFi, information is sent and received over two or more antennas simultaneously using the same frequency band, thus providing greater range and increasing throughput while maintaining compatibility with legacy IEEE 802.11a/b/g/n devices.

The BCM43526 supports the IEEE 802.11ac draft standard, which provides increased data rates in the 5 GHz band.

The BCM43526 architecture with its fully integrated dual-band radio transceiver supports two antennas for data rates up to 867 Mbps. State-of-the-art security is provided by industry standardized system support for WPA™ WPA2™(802.11i), and hardware accelerated AES encryption/ decryption, coupled with TKIP and IEEE 802.1X support. Embedded hardware acceleration enables increased system performance and significant reduction in host-CPU utilization in both client and access point configurations. The BCM43526 also supports the widely accepted and deployed Broadcom Wi-Fi WPS for ease-of-use.

FEATURES

- IEEE 802.11ac Draft compliant.
- Two-stream spatial multiplexing up to 867 Mbps data rate.
- Supports 20, 40, and 80 MHz channels with optional SGI (256 QAM modulation).
- Support for STBC and LDPC, in both TX and RX for increased wireless coverage.
- Greenfield, mixed mode, and legacy modes supported.
- Full IEEE 802.11a/b/g/n legacy compatibility with enhanced performance.
- USB 2.0 host interface for USB dongle & media applications supporting up to 480Mbps data rates
- Supports WHQL certified drivers for Windows® 8, Windows 7, Vista 32- and 64-bit, and Windows XP.
- Comprehensive wireless network security support that includes WPA, WPA2, and AES encryption/ decryption.
- Available in 12 × 12 mm, 108-pin QFN package.

APPLICATIONS

- USB add-in client dongles for PC desktop and notebook applications.
- Digital TV & USB Set-top Box solutions

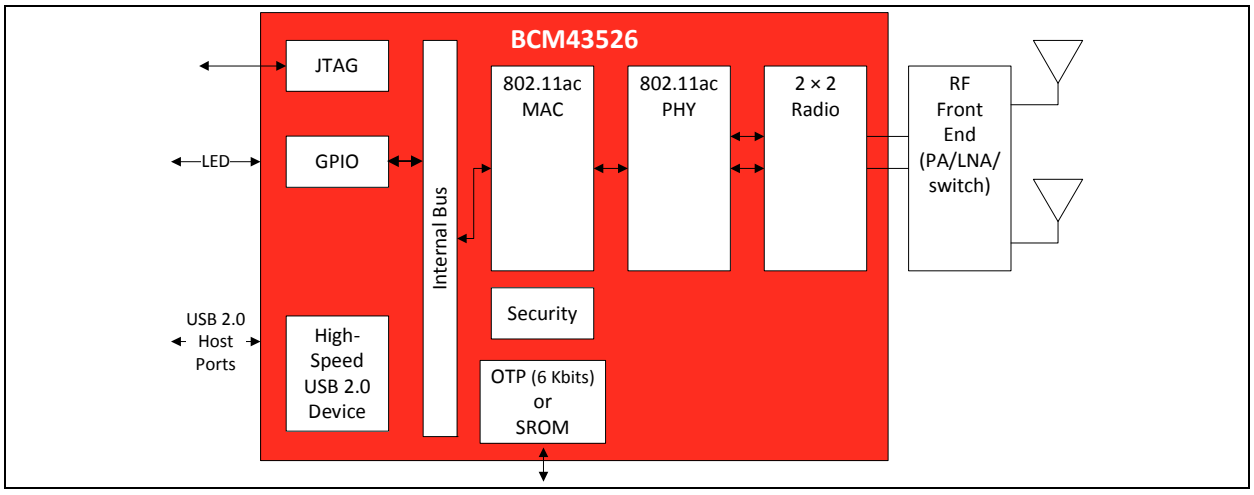

Figure 1: BCM43526 Block Diagram

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Revision History

Revision	*Date*	*Change Description*
43526-DS101-R	10/24/12	**Updated:** • Table 9: “WLAN 2.4 GHz Receiver Performance Specifications,” on page 32 • Table 10: “WLAN 2.4 GHz Transmitter Performance Specifications,” on page 37 • Table 11: “WLAN 5 GHz Receiver Performance Specifications,” on page 38 • Table 12: “WLAN 5 GHz Transmitter Performance Specifications,” on page 41 • Table 13: “General Spurious Emissions Specifications,” on page 42 • Table 14: “Power-Up Timing Parameters,” on page 43
43526-DS100-R	04/13/12	Initial release

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Table of Contents

List of Figures

List of Tables

About This Document

Purpose and Audience

This data sheet provides details about the functional, operational, and electrical characteristics of the Broadcom® BCM43526. It is intended for hardware design, application, and OEM engineers.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a comprehensive list of acronyms and other terms used in Broadcom documents, go to http://www.broadcom.com/press/glossary.php.

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

Section 1: Introduction

The BCM43526 is the latest innovative chip from Broadcom and is based on IEEE 802.11ac Draft. The chip is designed to take current WLAN systems to the next level of higher performance and greater range with Multiple Input Multiple Output (MIMO) technology, as shown in Figure 2. IEEE 802.11ac Draft more than doubles the spectral efficiency compared to that of current IEEE 802.11a/g WLANs.

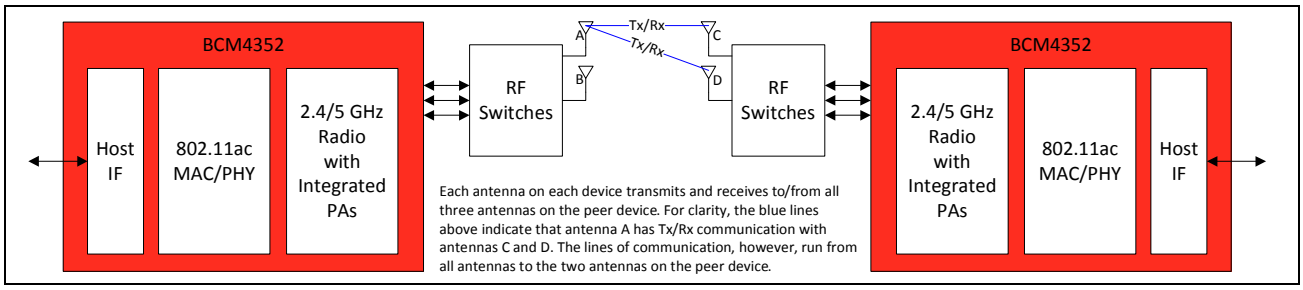


Figure 2: MIMO System Diagram Showing 2 × 2 Antenna Configuration

Employing a native 32-bit bus with direct memory access (DMA) architecture, the BCM43526 offers significant performance improvements in both transfer rates and CPU utilization.

Figure 3 shows a block diagram of the device.

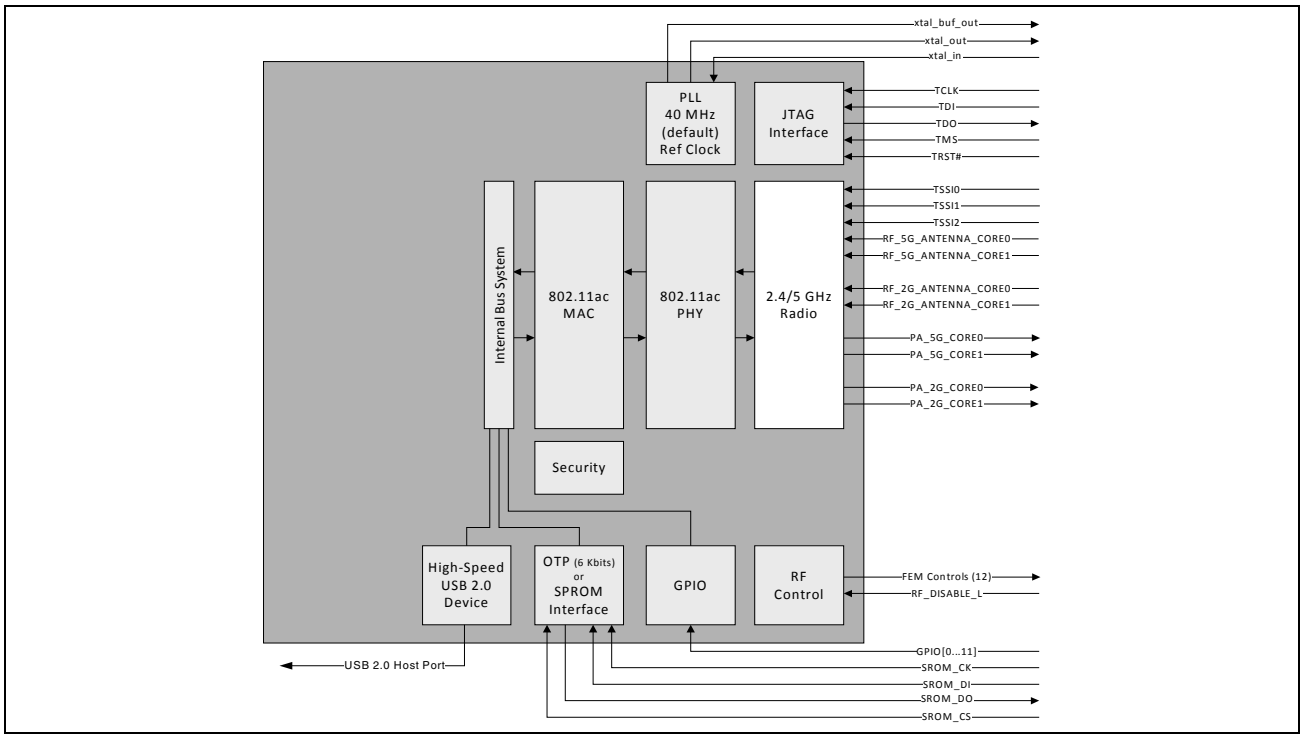


Figure 3: BCM43526 Functional Block Diagram

Section 2: Functional Description

Global Functions

Power Management

The BCM43526 has been designed with the stringent power consumption requirements of battery-powered hosts in mind. All areas of the chip design were scrutinized to help reduce power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages.

Additionally, the BCM43526 includes an advanced Power Management Unit (PMU). The PMU provides significant power savings by putting the BCM43526 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters in the PMU are used to turn on/off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

Voltage Regulators

Two Low-Dropout (LDO) regulators are integrated into the BCM43526: RFLDO and the PA VREF LDO.

Reset

A power-on or hard reset is initiated by an active low reset pulse on the perst_l Schmitt-triggered input pin. A 50 ms low pulse is recommended to guarantee that a sufficiently long reset is applied to all internal circuits, including integrated PHYs. The initialization process loads all pin configurable modes, resets all internal processes, and puts the device in the idle state. During initialization, the clock source input signal must be active, and all power supplies to the device (3.3V, 1.8V when applicable, and 1.2V) must be stable.

GPIO Interface

There are 12 General-Purpose I/O (GPIO) pins provided on the 12 × 12 package. GPIOs 8–11 are dedicated, whereas GPIOs 0–4 are multiplexed with the JTAG signal functions, GPIO 5 is multiplexed with the Power-On Reset, and GPIOs 6–7 are multiplexed with the UART signal functions. These pins can be used to attach to various external devices. Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. A programmable internal pull-up/pull-down resistor is included on each GPIO. If a GPIO output enable is not asserted, and the corresponding GPIO signal is not being driven externally, the GPIO state is determined by its programmable resistor.

OTP

The BCM43526 contains an on-chip One-time Programmable (OTP) area of 6 Kbit that can be used for non-volatile storage of WLAN information such as a MAC address and other hardware-specific parameters.

SPROM Interface (Optional)

Various hardware configuration parameters may be stored in an external SPROM instead of OTP. The SPROM is read by system software after device reset. In addition, customer-specific parameters may be stored in SPROM, depending on the specific board design.

The 4-wire SPROM interface supports 4 Kbit serial SPROMs by default. It also supports 16 Kbit serial SPROMs with the strapping option.

JTAG Interface

The BCM43526 supports the IEEE 1149.1 JTAG boundary-scan standard for testing the device packaging and PCB manufacturing.

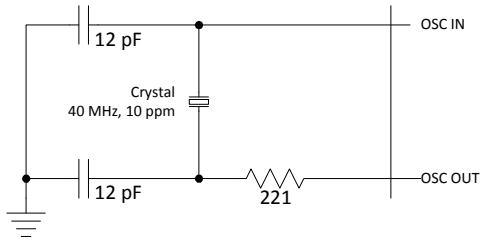
Crystal Oscillator

Table 1 lists the requirements for the crystal oscillator.

Table 1: Crystal Oscillator Requirements

Parameter	*Value*
Frequency	40 MHz (default) or 20 MHz
Mode	AT cut, fundamental
Load capacitance	12 pF
ESR	50Ω maximum
Frequency stability	±10 ppm at 25°C
Aging	±3 ppm/year max first year, ±1 ppm thereafter
Drive level	200 µW maximum
Shunt capacitance	< 5 pF

Figure 4 shows the recommended oscillator configuration.



NOTE:
Refer to reference schematics for design-specific details.

Figure 4: Recommended Oscillator Configuration

USB 2.0 Device Interface

To enable the USB 2.0 interface, the strapping pins must be configured as shown in Table 5 on page 33. The USB 2.0 device core provides the following features:

- Support for high speed at 480 Mbit/s or full speed at 12 Mbit/s operation
- USB 2.0 transceiver interface:
  - Data and clock recovery circuit
  - Bit stuffing and unstuffing; bit stuff error detection
  - SYNC/EOP generation and checking
  - Error detection and handling
  - Wake-up, resume, and suspend detection
- Endpoint management unit:
  - Manages USB traffic and DMA engine
- USB 2.0 protocol engine:
  - Parallel Interface Engine (PIE) between packet buffers and USB transceiver
  - Supports up to nine endpoints, including Configurable Control Endpoint 0
- Separate endpoint packet buffers with a 512-byte FIFO buffer each
- Host-to-device communication for bulk, control, and interrupt transfers
- Configuration/status registers

The various blocks in the USB 2.0 device core are shown in Figure 5.

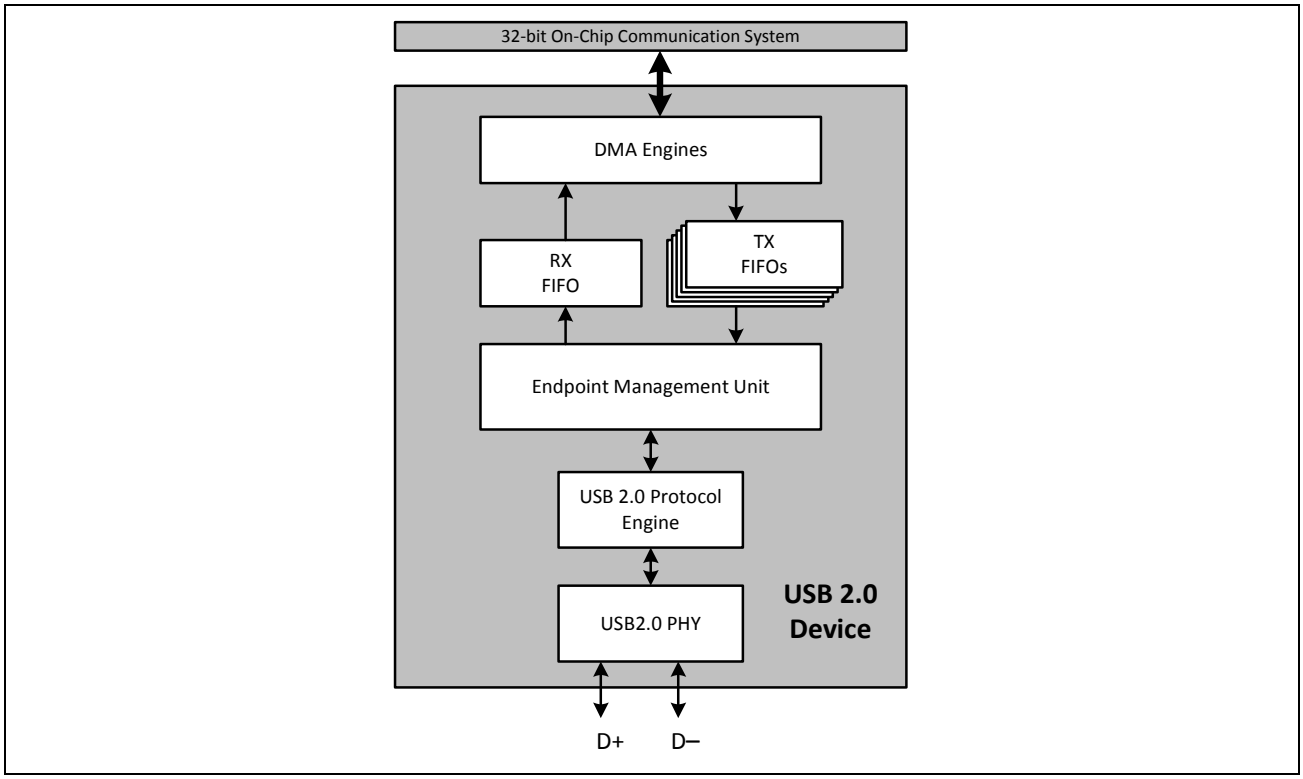


Figure 5: USB 2.0 Device Block Diagram

The USB 2.0 PHY handles the USB protocol and the serial signaling interface between the host and device. It is primarily responsible for data transmission and recovery. On the transmit side, data is encoded, along with a clock, using the NRZI scheme with bit stuffing to ensure that the receiver detects a transition in the data stream. A SYNC field that precedes each packet enables the receiver to synchronize the data and clock recovery circuits. On the receive side, the serial data is deserialized, unstuffed, and checked for errors. The recovered data and clock are then shifted to the clock domain that is compatible with the internal bus logic.

The endpoint management unit contains the PIE control logic and the endpoint logic. The PIE interfaces between the packet buffers and the USB transceiver. It handles Packet Identification (PID), USB packets, and transactions.

The endpoint logic contains nine uniquely addressable endpoints. These endpoints are the source or sink of communication flow between the host and the device. Endpoint zero is used as a default control port for both the input and output directions. The USB system software uses this default control method to initialize and configure the device information and allows USB status and control access. Endpoint zero is always accessible after a device is attached, powered, and reset.

Endpoints are supported by 512-byte FIFO buffers, one for each IN endpoint and one shared by all OUT endpoints. Both TX and RX data transfers support a DMA burst of 4, which guarantees low latency and maximum throughput performance. The RX FIFO can never overflow by design. The maximum USB packet size cannot be more than 512 bytes.

Serial Flash Interface

An option to use external serial flash is available when USB 2.0 operation is selected. The SPROM and SFLASH interfaces are pin-multiplexed and are not available simultaneously.

IEEE 802.11ac Draft MAC Description

The IEEE 802.11ac Draft MAC features include:

- Enhanced MAC for supporting 802.11ac Draft features
- Programmable Access Point (AP) or Station (STA) functionality
- Programmable Independent Basic Service Set (IBSS) or infrastructure mode
- Aggregated MPDU (MAC Protocol Data Unit) support for High-throughput (HT)
- Passive scanning
- Network Allocation Vector (NAV), Interframe Space (IFS), and Timing Synchronization Function (TSF) functionality
- RTS/CTS procedure
- Transmission of response frames (ACK/CTS)
- Address filtering of receive frames as specified by IBSS rules
- Multirate support
- Programmable Target Beacon Transmission Time (TBTT), beacon transmission/cancellation and programmable Announcement Traffic Indication Message (ATIM) window
- CF conformance: Setting NAV for neighborhood Point Coordination Function (PCF) operation
- Security through a variety of encryption schemes including WEP, TKIP, AES, WPA, WAP2, and IEEE 802.1X
- Power management
- Statistics counters for MIB support

The MAC core supports the transmission and reception of sequences of packets, together with related timing, without any packet-by-packet driver interaction. Time-critical tasks requiring response times of only a few milliseconds are handled in the MAC core. This achieves the required timing on the medium while keeping the host driver easier to write and maintain. Also, incoming packets are buffered in the MAC core, which allows the MAC driver to process them in bursts, enabling high bandwidth performance.

The MAC driver interacts with the MAC core to prepare queues of packets to transmit and to analyze and forward received packets to upper software layers. The internal blocks of the MAC core are connected to a Programmable State Machine (PSM) through the host interface that connects to the internal bus (see Figure 6 on page 15).

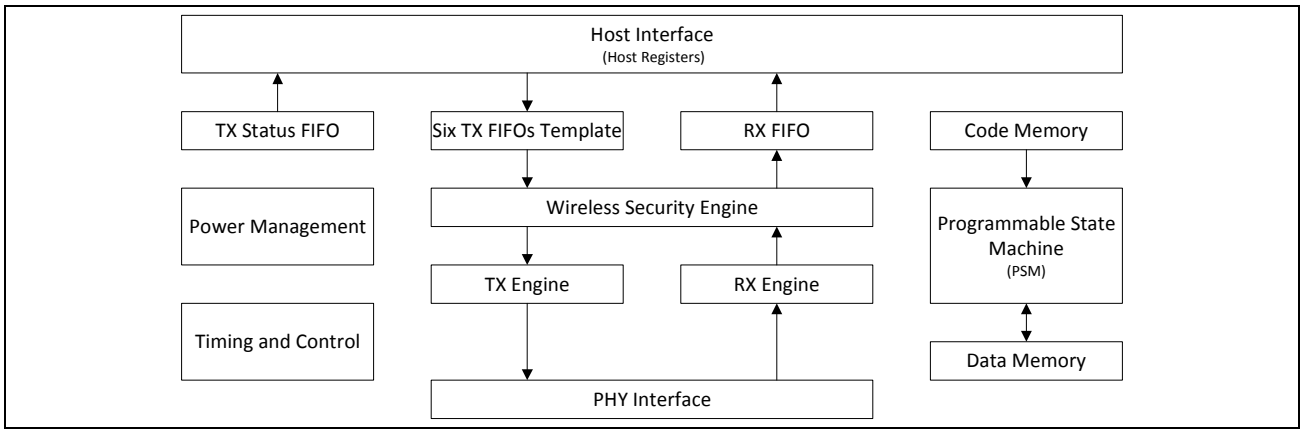


Figure 6: Enhanced MAC Block Diagram

The host interface consists of registers for controlling and monitoring the status of the MAC core and interfacing with the TX/RX FIFOs. For transmit, a total of 512 KB of buffer memory is available that can be dynamically allocated to six transmit queues plus template space for beacons, ACKs, and probe responses. Whenever the host has a frame to transmit, the host queues the frame into one of the transmit FIFOs with a TX descriptor containing TX control information. The PSM schedules the transmission on the medium depending on the frame type, transmission rules in IEEE 802.11 protocol, and the current medium occupancy scenario. After the transmission is completed, a TX status is returned to the host, informing the host of the result that got transmitted.

The MAC contains two RX channels that each have 20 KB of buffer memory. Whenever a frame is received, the frame is sent to the host along with an RX descriptor that contains additional information about the frame reception conditions.

The power management block maintains the information regarding the power management state of the core (and the associated STAs in case of an AP) to help in dynamic decisions by the core regarding frame transmission.

The wireless security engine performs the required encryption/decryption on the TX/RX frames. This block supports separate transmit and receive keys with four shared keys and 50 link-specific keys. The link-specific keys are used to establish a secure link between any two STAs, with the required key being shared between only those two STAs, hence excluding all of the other STAs in the same network from deciphering the communication between those two STAs. The wireless security engine supports the following encryption schemes that can be selected on a per-destination basis:

- None: The wireless security engine acts as a pass-through
- WEP: 40-bit secure key and 24-bit IV as defined in IEEE Std. 802.11-2007
- WEP128: 104-bit secure key and 24-bit IV
- TKIP: IEEE Std. 802.11-2007
- AES: IEEE Std. 802.11-2007

The transmit engine is responsible for the byte flow from the TX FIFO to the PHY interface through the encryption engine and the addition of an FCS (CRC-32) as required by IEEE 802.11-2007. Similarly, the receive engine is responsible for byte flow from the PHY interface to the RX FIFO through the decryption engine and for detection of errors in the RX frame.

The timing block performs the TSF, NAV, and IFS functionality as described in IEEE Std. 802.11-2007.

The Programmable State Machine (PSM) coordinates the operation of different hardware blocks required for both transmission and reception. The PSM also maintains the statistics counters required for MIB support.

IEEE 802.11ac Draft PHY Description

The PHY features include:

- Programmable data rates from MCS 0–23 and MCS 32 in 20 MHz and 40 MHz channels, and VHTMCS 0–9 in 20 MHz, 40 MHz, and 80 MHz channels, as specified in 802.11ac Draft.
- Support for Short Guard Interval (SGI), Space-Time Block Coding (STBC), and Low-Density Parity Check Coding (LDPC).
- All scrambling, encoding, forward error correction, and modulation in the transmit direction, and inverse operations in the receive direction.
- Advanced digital signal processing technology for best-in-class receive sensitivity.
- Both long and optional short preambles of IEEE 802.11b.
- Resistance to multipath (>250 nanoseconds RMS delay spread) with maximal ratio combining for high throughput and range performance, including improved performance in legacy mode over existing IEEE 802.11a/b/g solutions.
- Automatic Gain Control (AGC).
- Available per-packet channel quality and signal strength measurements.

The dual PHYs integrated in the BCM43526 provide baseband processing at all mandatory data rates specified in the 802.11n specification up to 450 Mbps, at all mandatory and optional MCS specified in the 802.11ac Draft up to 1.3 Gbps, and the legacy rates specified in IEEE 802.11a/b/g including 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54 Mbps. This core acts as an intermediary between the MAC and the dual-band 2.4/5 GHz radio, converting back and forth between packets and baseband waveforms.

Dual-Band Radio Transceiver

Integrated into the BCM43526 is Broadcom's world-class dual-band radio transceiver that ensures low-power consumption and robust communications for applications operating in the 2.4 and 5 GHz bands. Channel bandwidths of 20 MHz, 40 MHz, and 80 MHz are supported as specified in 802.11ac Draft.

Receiver Path

The BCM43526 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. The excellent noise figure of the receiver makes an external LNA unnecessary.

Transmitter Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band or the 5 GHz U-NII bands, respectively.

Calibration

The BCM43526 features dynamic on-chip calibration, eliminating process variation across components. This enables the device to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation.

Section 3: Pin Assignments

This section contains pin assignments and ballout information for the BCM43526 108-pin package. There is one package:

- 12 × 12, 108 pins for access point, router, and media applications.

BCM43526 QFN Pin Assignments

Figure 7 on page 19 shows pin assignments for the 108-pin QFN package.

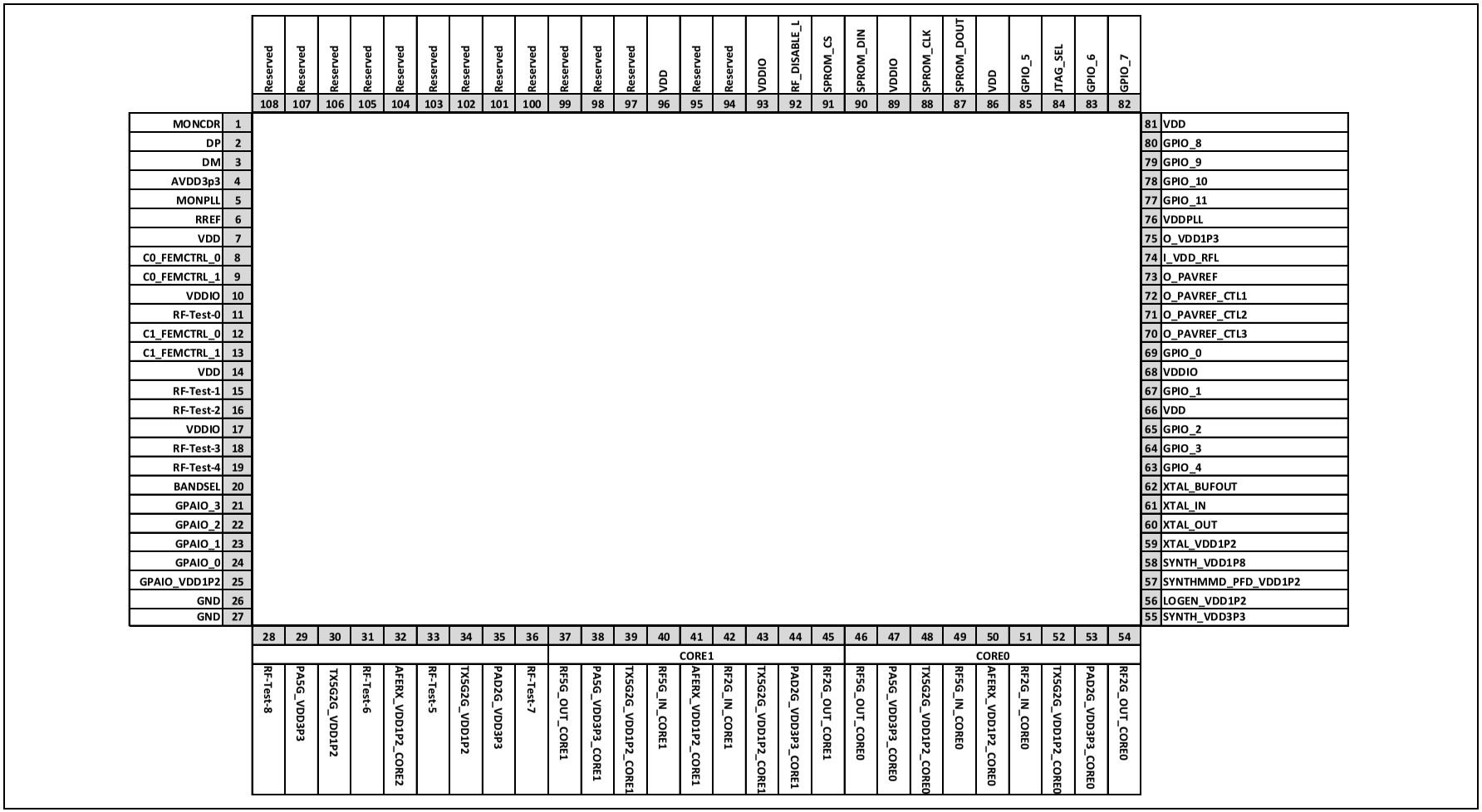


Figure 7: 108-Pin (12 × 12) QFN Package

Signals by Pin Number

Table 2: 108-Pin (12 × 12) Pins and Signals

Pin	Signal
1	MONCDR
2	DP
3	DM
4	AVDD3p3
5	MONPLL
6	RREF
7	VDD
8	C0_FEMCTRL_0
9	C0_FEMCTRL_1
10	VDDIO
11	RF-Test-0
12	C1_FEMCTRL_0
13	C1_FEMCTRL_1
14	VDD
15	RF-Test-1
16	RF-Test-2
17	VDDIO
18	RF-Test-3
19	RF-Test-4
20	BANDSEL
21	GPAIO_3
22	GPAIO_2
23	GPAIO_1
24	GPAIO_0
25	GPAIO_VDD1P2
26	GND
27	GND
28	RF-Test-8
29	PA5G_VDD3P3_CORE2
30	TX5G2G_VDD1P2_CORE2
31	RF-Test-6
32	AFERX_VDD1P2_CORE2
33	RF-Test-5
34	TX5G2G_VDD1P2_CORE2
35	PAD2G_VDD3P3_CORE2

Table 2: 108-Pin (12 × 12) Pins and Signals (Cont.)

Pin	Signal
36	RF-Test-7
37	RF5G_OUT_CORE1
38	PA5G_VDD3P3_CORE1
39	TX5G2G_VDD1P2_CORE1
40	RF5G_IN_CORE1
41	AFERX_VDD1P2_CORE1
42	RF2G_IN_CORE1
43	TX5G2G_VDD1P2_CORE1
44	PAD2G_VDD3P3_CORE1
45	RF2G_OUT_CORE1
46	RF5G_OUT_CORE0
47	PA5G_VDD3P3_CORE0
48	TX5G2G_VDD1P2_CORE0
49	RF5G_IN_CORE0
50	AFERX_VDD1P2_CORE0
51	RF2G_IN_CORE0
52	TX5G2G_VDD1P2_CORE0
53	PAD2G_VDD3P3_CORE0
54	RF2G_OUT_CORE0
55	SYNTH_VDD3P3
56	LOGEN_VDD1P2
57	SYNTHMMD_PFD_VDD1P2
58	SYNTH_VDD1P8
59	XTAL_VDD1P2
60	XTAL_OUT
61	XTAL_IN
62	XTAL_BUFOUT
63	GPIO_4
64	GPIO_3
65	GPIO_2
66	VDD
67	GPIO_1
68	VDDIO
69	GPIO_0
70	RF_Test_9

Table 2: 108-Pin (12 × 12) Pins and Signals (Cont.)

Pin	Signal
71	O_PAVREF_CTL2
72	O_PAVREF_CTL1
73	O_PAVREF
74	I_VDD_RFL
75	O_VDD1P3
76	VDDPLL
77	GPIO_11
78	GPIO_10
79	GPIO_9
80	GPIO_8
81	VDD
82	GPIO_7
83	GPIO_6
84	JTAG_SEL
85	GPIO_5
86	VDD
87	SPROM_DOUT
88	SPROM_CLK
89	VDDIO

Table 2: 108-Pin (12 × 12) Pins and Signals (Cont.)

Pin	Signal
90	SPROM_DIN
91	SPROM_CS
92	RF_DISABLE_L
93	VDDIO
94	Reserved
95	Reserved
96	VDD
97	Reserved
98	Reserved
99	Reserved
100	Reserved
101	Reserved
102	Reserved
103	Reserved
104	Reserved
105	Reserved
106	Reserved
107	Reserved
108	RVDD

Section 4: Signal and Pin Descriptions

Package Signal Descriptions

The signal name, type, and description of each pin in the BCM43526 108-pin QFN package are listed in Table 3. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any. See also Table 4 on page 27 for resistor strapping options.

Table 3: Signal Descriptions

Signal Name	*Pin No.*	*Type*	*Description*
Crystal Oscillator			
XTAL_IN	61	I	XTAL oscillator input. Connect a 20 MHz 10 ppm crystal between the xtal_in and xtal_out pins.
XTAL_OUT	60	O	XTAL oscillator output
XTAL_BUF_OUT	62	O	Buffered XTAL output
SPROM Interface			
SPROM_CLK	88	O (4 mA)	Serial data clock output. This pin is multiplexed with: • GPIO_13 • btcx_bt_pri_status, Bluetooth coexistence output, status
SPROM_CS	91	O (4 mA)	SPROM chip select
SPROM_DIN	90	I	SPROM data in. This pin is multiplexed with: • GPIO_15 • btcx_coex_status2, Bluetooth coexistence output, status 2
SPROM_DOUT	87	O (4 mA)	SPROM data out. This pin is multiplexed with GPIO_14
USB Interface			
DP	2	I/O	USB (Host) data plus. Positive terminal of the USB transceiver.
DM	3	I/O	USB (Host) data minus. Negative terminal of the USB transceiver.
RREF	6	I/O	USB analog test. Bandgap reference resistor. Connect to a parallel 4.02K ±1% resistor and a 100 pF capacitor to ground. Refer to the reference schematic for more details.
MONCDR	1	I/O	CDR monitoring test pin. Do not connect anything to this pin.
MONPLL	5	I/O	Pin used for PLL, BG, CDR.

Table 3: Signal Descriptions (Cont.)

Signal Name	Pin No.	Type	Description
RF Control Interface			
C0_FEMCTRL_0	8	O	TR switch controls for core 0. These pins are also used as strapping options (see Table 4 on page 27).
C0_FEMCTRL_1	9		
C1_FEMCTRL_0	12	O	TR Switch controls for core 1. These pins are also used as strapping options (see Table 4 on page 27).
C1_FEMCTRL_1	13		
BANDSEL	20	I	RF band select. This pin is also used as a strapping option (see Table 4 on page 27).
RF_DISABLE_L	92	I	RF disable. When asserted, disables the internal radio and shuts off everything except the crystal oscillator.
RF Signal Interface			
RF2G_IN_CORE0	51	I	Core 0 RF receive input, 2.4 GHz band
RF2G_IN_CORE1	42	I	Core 1 RF receive input, 2.4 GHz band
RF5G_IN_CORE0	49	I	Core 0 RF receive input, 5 GHz band
RF5G_IN_CORE1	40	I	Core 1 RF receive input, 5 GHz band
RF2G_OUT_CORE0	54	I	Core 0 RF transmit output, 2.4 GHz band
RF2G_OUT_CORE1	45	I	Core 1 RF transmit output, 2.4 GHz band
RF5G_OUT_CORE0	46	I	Core 0 RF transmit output, 5 GHz band
RF5G_OUT_CORE1	37	I	Core 1 RF transmit output, 5 GHz band
GPAIO_0	24	I	TSSI input from power detector
GPAIO_1	23	I	TSSI input from power detector
GPAIO_2	22	I	TSSI input from power detector
GPAIO_3	21	I	TSSI input from power detector
RF Test Pins			
RF-Test-0	11	–	RF Test pin. This pin is also used as strapping options (see Table 4 on page 27).
RF-Test-1	15	–	RF Test pin
RF-Test-2	16	–	RF Test pin. This pin is also used as strapping options (see Table 4 on page 27).
RF-Test-3	18	–	RF Test pin
RF-Test-4	19	–	RF Test pin. This pin is also used as strapping options (see Table 4 on page 27).
RF-Test-5	33	–	RF Test pin
RF-Test-6	31	–	RF Test pin
RF-Test-7	36	–	RF Test pin
RF-Test-8	28	–	RF Test pin
RF-Test-9	70	–	RF Test pin

Table 3: Signal Descriptions (Cont.)

Signal Name	*Pin No.*	*Type*	*Description*
JTAG Interface			
GPIO_0	69	I/O	JTAG Reset Input. Resets the JTAG Controller. If not used, this pin should be pulled low via a 1 kΩ resistor. This pin is multiplexed with: • GPIO_0 • btcx_wlan_act, Bluetooth coexistence output, WLAN active
GPIO_1	67	I/O	JTAG Test Clock Input. Used to synchronize JTAG control and data transfers. If not used, this pin should be pulled low via a 1 kΩ resistor. This pin is multiplexed with: • GPIO_1 • btcx_bt_active, Bluetooth coexistence output, Bluetooth active
GPIO_2	65	I/O	JTAG Test Data Input. Serial data input to the JTAG TAP controller. Sampled on the rising edge of TCK. If not used, it may be left unconnected. This pin is multiplexed with: • GPIO_3 • bt_coex_status2, Bluetooth coexistence output, status 2
GPIO_3	64	I/O	JTAG Test Data Output. Serial data output from the JTAG TAP controller. Sampled on the rising edge of TCK. If not used, it may be left unconnected. This pin is multiplexed with: • GPIO_2 • btcx_bt_iodisable, Bluetooth coexistence output, I/O disable
GPIO_4	63	I/O	JTAG Mode Select Input. Single-control input to the JTAG TAP controller used to traverse the test logic state machine. Sampled on the rising edge of TCK. If not used, it may be left unconnected. This pin is multiplexed with: • GPIO_4 • ext_bt_shd0, Bluetooth shared antenna 0 control
JTAG_SELECT	84	I	JTAG Select
GPIO Interface			
GPIO_5	85	I/O (8 mA)	GPIO_5, general-purpose I/O: This pin is also multiplexed with: • por_l, External Power-On Reset (POR) input. • ext_bt_shd1, Bluetooth shared antenna 1 control.
GPIO_6	83	I/O	GPIO_6, general-purpose I/O: This pin is also multiplexed with ext_lna_0_g, external 2.4 GHz LNA control for core 0.
GPIO_7	82	I/O	GPIO_7, general-purpose I/O: This pin is also multiplexed with ext_lna_1_g, external 2.4 GHz LNA control for core 1.
GPIO_8	80	I/O	GPIO_8, general-purpose I/O
GPIO_9	79	I/O	GPIO_9, general-purpose I/O: This pin is also multiplexed with ext_lna_0_a, external 5 GHz LNA control for core 0.

Table 3: Signal Descriptions (Cont.)

Signal Name	*Pin No.*	*Type*	*Description*
GPIO_10	78	I/O	GPIO_10, general-purpose I/O: This pin is also multiplexed with ext_lna_1_a, external 5 GHz LNA control for core 1.
GPIO_11	77	I/O	GPIO_11, general-purpose I/O
Power and Ground			
VDD	7, 14, 66, 81, 86, 96	PWR	1.2V supply input for the core logic
VDDIO	10, 17, 68, 89, 93	PWR	3.3V supply input for digital I/O
GPAIO_VDD1P2	25	PWR	1.2V supply input for the analog I/O logic
AFERX_VDD1P2_CORE0	50	PWR	1.2V supply input for LNA
AFERX_VDD1P2_CORE1	41	PWR	1.2V supply input for LNA
AFERX_VDD1P2_CORE2	32	PWR	1.2V supply input for LNA
TX5G2G_VDD1P2_CORE0	48, 52	PWR	1.2V supply input for RF
TX5G2G_VDD1P2_CORE1	39, 43	PWR	1.2V supply input for RF
TX5G2G_VDD1P2	30, 34	PWR	1.2V supply input for the RF
AVDD3p3	4	PWR	3.3V supply input
LOGEN_VDD1P2	56	PWR	Analog 1.2V supply input
SYNTHMMD_PFD_VDD1P2	57	PWR	Analog 1.2V supply input
SYNTH_VDD1P8	58	PWR	Analog 1.8V supply input
SYNTH_VDD3P3	55	PWR	Analog 3.3V supply input
XTAL_VDD1P2	59	O	Crystal LDO reference: Decouple to ground (see reference schematic)
VDDPLL	75	PWR	Analog 1.2V supply input
PA5G_VDD3P3_CORE0	47	PWR	Filtered 3.3V input to internal PA of 5 GHz
PA5G_VDD3P3_CORE1	38	PWR	Filtered 3.3V input to internal PA of 5 GHz
PA5G_VDD3P3	29	PWR	Filtered 3.3V input to internal of 5 GHz PA
PA2G_VDD3P3_CORE0	53	PWR	Filtered 3.3V input to internal PA of 2.4 GHz
PA2G_VDD3P3_CORE1	44	PWR	Filtered 3.3V input to internal PA of 2.4 GHz
PA2G_VDD3P3	35	PWR	Filtered 3.3V input to internal 2.4 GHz PA
O_PAVREF_CTL1	72	PWR	PA LDO regulated output 1
O_PAVREF_CTL2	71	PWR	PA LDO regulated output 2
O_PAVREF	73	PWR	PA LDO reference, decouple to ground (see reference schematic)
I_VDD_RFL	74	PWR	3.3V input to RF LDO
O_VDD1P3	75	O	RF LDO reference supply
GND	26, 27	GND	Ground

Table 3: Signal Descriptions (Cont.)

Signal Name	*Pin No.*	*Type*	*Description*
Reserved			
Reserved	94, 95, 97, 98, 99, 100 101, 102, 103, 104, 105, 106, 107, 108	I/O	Reserved

Strapping Options

The pins listed in Table 4 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs within a few milliseconds following internal POR or deassertion of external POR. After POR, each pin assumes the function specified in the signal descriptions table. Each pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND—use 10 kΩ or less (refer to the reference board schematics for further details).

Table 4: Strapping Options[a]

Signal Name	*Mode*	*Default*	*Description*
C0_FEMCTRL_1	Crystal select	PU	0: 20 MHz XTAL selected 1: 40 MHz XTAL selected
C1_FEMCTRL_0, RF-Test-0	SROM Size	PD,PU	0, 1: 4K SROM size 1, 0: 16K SROM size
C1_FEMCTRL_1	Boot Method	PU	0: Boot from SRAM 1: Boot from ROM
RE-Test-2	OTP select	PD	0: OTP not present 1: OTP present
RF-Test-4	Serial flash select	PU	0: Atmel® serial flash 1: ST® serial flash
BANDSEL	Serial flash present	PD	0: Serial flash not present 1: Serial flash present
GPIO[7,6]	Internal clock select	PU,PU	1, 1: HT clock select 1, 0: ALP clock select
GPIO8	USB interface select	PD	0: Reserved 1: USB select

a. These functions are controlled by the strapping option and the driver. These pins should be strapped as shown in the appropriate Broadcom reference board schematic.

Section 5: Electrical Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 5: Absolute Maximum Ratings

Rating	*Symbol*	*Minimum*	*Maximum*	*Unit*
DC supply voltage for core	VDDC	–0.5	TBD	V
DC supply voltage for I/O	VDDO	–0.5	+3.8	V
Voltage on any input or output pin	V_{IMAX}, V_{IMIN}	–0.5	+3.8[a]	V
Ambient Temp (Operating)	T_A	0	+70	°C
Operating Junction Temperature	T_J	–	+125	°C
Operating Humidity	–	–	85	%
Storage Temperature	T_{STG}	–40	+125	°C
Storage Humidity	–	–	60	%
ESD Protection (HBM)	V_{ESD}	–	2000	V

a. The max voltage requirement is to not exceed VDDO + 0.5V when VDDO < 3.3V.

Recommended Operating Conditions and DC Characteristics

Table 6: Recommended Operating Conditions and DC Characteristics

		Value			
Element	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
DC supply voltage for I/O	VDDO	3.0	3.3	3.63	V
DC supply voltage for core and 1.2V analog	VDD12	1.16	1.2	1.24	V
Input low voltage (VDDO = 3.3V)	V_{IL}	–	–	0.8	V
Input high voltage (VDDO = 3.3V)	V_{IH}	2.0	–	–	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	VDDO – 0.4V	–	–	V

Current Consumption

Table 7: BCM43526 Current Consumption

Item	***1.2V***	***3.3V***	***Units***
Radio disabled state	TBD	TBD	mA
Idle and associated state, PM2 mode	TBD	TBD	mA
Active state, TX mode, maximum throughput, average current	TBD	TBD	mA
Active state, RX mode, maximum throughput, average current	TBD	TBD	mA
Active state, TX mode, maximum throughput, peak current	TBD	TBD	mA
Active state, RX mode, maximum throughput, peak current	TBD	TBD	mA

Note: These power consumption numbers were derived under the following nominal conditions:

- Typical corner silicon
- Nominal temperature (25°C)
- Nominal voltages

Section 6: RF Specifications

Introduction

The BCM43526 includes an integrated dual-band direct conversion radio that supports either the 2.4 GHz band or the 5 GHz band. This section describes the RF characteristics of the 2.4 GHz and 5 GHz portions of the radio.

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply for the conditions specified in Table 5: "Absolute Maximum Ratings," on page 28 and Table 6: "Recommended Operating Conditions and DC Characteristics," on page 29. Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

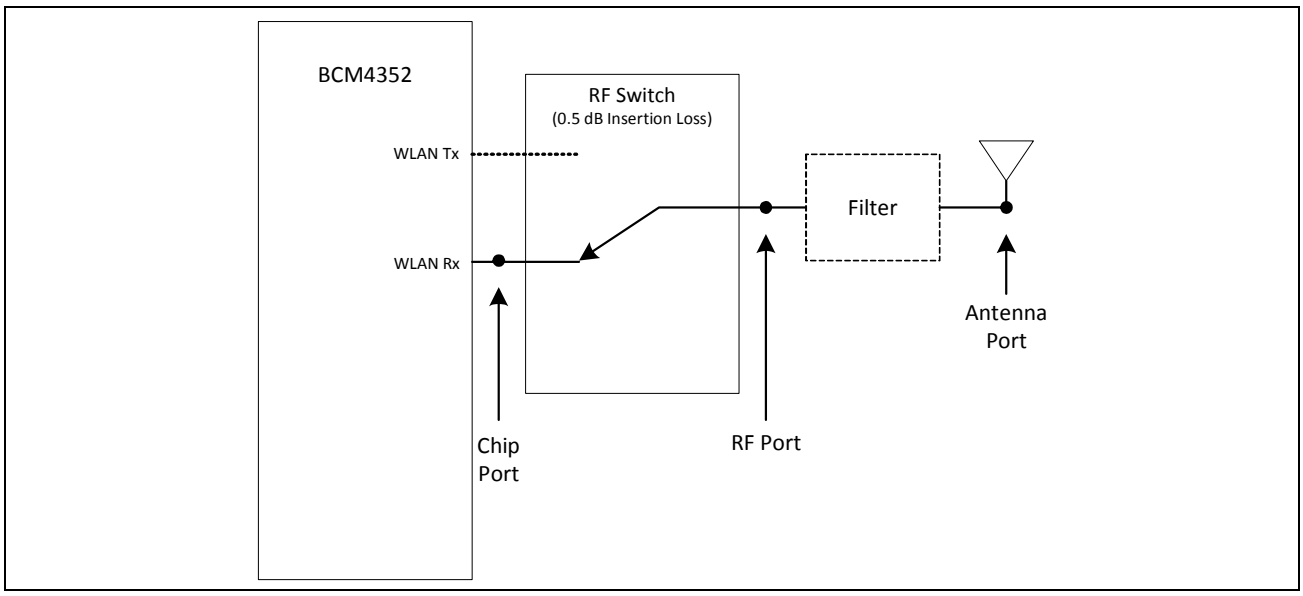


Figure 8: Port Locations

Note: All WLAN specifications are measured at the chip port, unless otherwise specified.

2.4 GHz Band General RF Specifications

Table 8: 2.4 GHz Band General RF Specifications

Item	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
Tx/Rx switch time	Including TX ramp down	–	–	5	µs
Rx/Tx switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 9 are measured at the chip port, unless otherwise specified. All data is preliminary and subject to change.

Table 9: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	*Condition/Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
Frequency range	–	2400	–	2500	MHz
IEEE 802.11b RX sensitivity (8% PER for 1024 octet PSDU)[a]	1 Mbps DSSS	–	–98	–	dBm
	2 Mbps DSSS	–	–97	–	dBm
	5.5 Mbps DSSS	–	–94	–	dBm
	11 Mbps DSSS	–	–91	–	dBm
IEEE 802.11g RX sensitivity (10% PER for 1024 octet PSDU)[a]	6 Mbps OFDM	–	–96	–	dBm
	9 Mbps OFDM	–	–94	–	dBm
	12 Mbps OFDM	–	–93	–	dBm
	18 Mbps OFDM	–	–91	–	dBm
	24 Mbps OFDM	–	–87	–	dBm
	36 Mbps OFDM	–	–84	–	dBm
	48 Mbps OFDM	–	–79	–	dBm
	54 Mbps OFDM	–	–78	–	dBm

Table 9: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
IEEE 802.11n RX sensitivity (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 15	−64	−70	–	dBm
	MCS 8	−82	−90	–	dBm
	MCS 7	−64	−76	–	dBm
	MCS 6	−65	−77	–	dBm
	MCS 5	−66	−79	–	dBm
	MCS 4	−70	−80	–	dBm
	MCS 3	−74	−87	–	dBm
	MCS 2	−77	−90	–	dBm
	MCS 1	−79	−93	–	dBm
	MCS 0	−82	−95	–	dBm
	40 MHz channel spacing for all MCS rates				
	MCS 15	−54	−65	–	dBm
	MCS 8	−56	−67	–	dBm
	MCS 7	−61	−73	–	dBm
	MCS 6	−62	−75	–	dBm
	MCS 5	−63	−76	–	dBm
	MCS 4	−67	−81	–	dBm
	MCS 3	−71	−84	–	dBm
	MCS 2	−74	−88	–	dBm
	MCS 1	−76	−90	–	dBm
	MCS 0	−79	−93	–	dBm
IEEE 802.11ac (Nss = 3) RX sensitivity (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS9	–57	−69	–	dBm
	MCS 8	−59	−71	–	dBm
	MCS 7	−64	−76	–	dBm
	MCS 6	−65	−76	–	dBm
	MCS 5	−66	−78	–	dBm
	MCS 4	−70	−82	–	dBm
	MCS 3	−74	−86	–	dBm
	MCS 2	−77	−89	–	dBm
	MCS 1	−79	−91	–	dBm
	MCS 0	−82	−94	–	dBm

Table 9: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
IEEE 802.11ac RX sensitivity (10% PER for 4096 octet PSDU)[a,b.] Defined for default parameters: GF, 800 ns GI, and non-STBC.	40 MHz channel spacing for all MCS rates				
	MCS 9	−54	−68	–	dBm
	MCS 8	−56	−69	–	dBm
	MCS 7	−61	−73	–	dBm
	MCS 6	−62	−73	–	dBm
	MCS 5	−63	−75	–	dBm
	MCS 4	−67	−80	–	dBm
	MCS 3	−71	−83	–	dBm
	MCS 2	−74	−86	–	dBm
	MCS 1	−76	−88	–	dBm
	MCS 0	−79	−92	–	dBm
	80 MHz channel spacing for all MCS rates				
	MCS 9	−51	−64	–	dBm
	MCS 8	−53	−65	–	dBm
	MCS 7	−58	−70	–	dBm
	MCS 6	−59	−70	–	dBm
	MCS 5	−60	−74	–	dBm
	MCS 4	−64	−76	–	dBm
	MCS 3	−68	−79	–	dBm
	MCS 2	−71	−83	–	dBm
	MCS 1	−73	−85	–	dBm
	MCS 0	−76	−88	–	dBm
In-band static CW jammer immunity (fc − 8 MHz < fcw < + 8 MHz)	Rx PER < 1%, 54 Mbps OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)	−80	–	–	dBm
Input In-Band IP3[a]	Maximum LNA gain	–	−15.5	–	dBm
	Minimum LNA gain	–	−1.5	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)	−3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)	−9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1024 octets)	−9.5	–	–	dBm
	@ MCS0–7 rates (10% PER, 4095 octets)	−9.5	–	–	dBm
LPF 3 dB Bandwidth	–	9	–	10	MHz

Table 9: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*		*Minimum*	*Typical*	*Maximum*	*Unit*
IEEE 802.11b adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	***Desired and interfering signal 30 MHz apart***					
	1 Mbps DSSS	–74 dBm	35	–	–	dB
	2 Mbps DSSS	–74 dBm	35	–	–	dB
	Desired and interfering signal 25 MHz apart					
	5.5 Mbps DSSS	–70 dBm	35	–	–	dB
	11 Mbps DSSS	–70 dBm	35	–	–	dB
IEEE 802.11g adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
IEEE 802.11n adjacent channel rejection MCS0–7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS7	–61 dBm	–2	–	–	dB
	MCS6	–62 dBm	–1	–	–	dB
	MCS5	–63 dBm	0	–	–	dB
	MCS4	–67 dBm	4	–	–	dB
	MCS3	–71 dBm	8	–	–	dB
	MCS2	–74 dBm	11	–	–	dB
	MCS1	–76 dBm	13	–	–	dB
	MCS0	–79 dBm	16	–	–	dB
IEEE 802.11ac adjacent channel rejection MCS0–9 (Difference between interfering and desired signal at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/Notes)	MCS9	–57 dBm	–9	–	–	dB
	MCS8	–59 dBm	–7	–	–	dB
	MCS7	–64 dBm	–2	–	–	dB
	MCS6	–65 dBm	–1	–	–	dB
	MCS5	–66 dBm	0	–	–	dB
	MCS4	–70 dBm	4	–	–	dB
	MCS3	–74 dBm	8	–	–	dB
	MCS2	–77 dBm	11	–	–	dB
	MCS1	–79 dBm	13	–	–	dB
	MCS0	–82 dBm	16	–	–	dB
Maximum receiver gain	–	–	95	–	–	dB
Gain control step	–	–	3	–	–	dB
RSSI accuracy[c]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB

Table 9: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
Return loss	Z_o = 50Ω, across the dynamic range	10	11.5	13	dB
Receiver cascaded noise figure	At maximum gain	–	4	–	

a. Derate by 1.5 dB for –30 °C to –10°C and 55°C to 85°C.
b. Sensitivity degradations for alternate settings in MCS modes. MM: 0.5 dB drop, SGI: 2 dB drop, and STBC: 0.75 dB drop.
c. The minimum and maximum values shown have a 95% confidence level.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 10 are measured at the chip port output, unless otherwise specified.

Table 10: WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Harmonic level (at –5 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	–8	–	dBm/1 MHz
	7.2–7.5 GHz	3rd harmonic	–	–18	–	dBm/1 MHz
Tx power at RF port for highest power level setting at 25°C and VBAT = 3.6V with spectral mask and EVM compliance[a, b]	802.11b (DSSS/CCK)	–9 dB	4	5.5	–	dBm
	OFDM, BPSK	–8 dB	4	5	–	dBm
	OFDM, QPSK	–13 dB	4	5	–	dBm
	OFDM, 16-QAM	–19 dB	2.5	4	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	1.5	2	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	0.5	2	–	dBm
	OFDM, 256-QAM (R = 3/4, VHT20)	–30 dB	TBD	–	–	dBm
	OFDM, 256-QAM (R = 5/6, VHT20)	–32 dB	TBD	–	–	dBm
Phase noise	37.4 MHz Crystal, Integrated from 10 kHz to 10 MHz		–	TBD	–	Degrees
Tx power control dynamic range	–		10	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at Chip port Tx Z_o = 50Ω			–	6	–	dB

a. Derate by 1.5 dB for temperatures less than –10°C or more than 55°C, or voltages less than 3.0V. Derate by 3.0 dB for voltages of less than 2.7V, or voltages of less than 3.0V at temperatures less than –10°C or greater than 55°C. Derate by 4.5 dB for –40°C to –30°C.

b. Tx power for Channel 1 and Channel 11 is specified by non-volatile memory parameters.

WLAN 5 GHz Receiver Performance Specifications

Note: The specifications in Table 11 are measured at the chip port input, unless otherwise specified.

Table 11: WLAN 5 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	4900	–	5845	MHz
IEEE 802.11a RX sensitivity (10% PER for 1000 octet PSDU)[a]	6 Mbps OFDM	–	−94.5	–	dBm
	9 Mbps OFDM	–	−93	–	dBm
	12 Mbps OFDM	–	−92	–	dBm
	18 Mbps OFDM	–	−89	–	dBm
	24 Mbps OFDM	–	−86	–	dBm
	36 Mbps OFDM	–	−83	–	dBm
	48 Mbps OFDM	–	−78	–	dBm
	54 Mbps OFDM	–	−76	–	dBm
IEEE 802.11n RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 15	–	−69	–	dBm
	MCS 8	–	−89	–	dBm
	MCS 7	–	−74	–	dBm
	MCS 6	–	−76	–	dBm
	MCS 5	–	−77	–	dBm
	MCS 4	–	−82	–	dBm
	MCS 3	–	−86	–	dBm
	MCS 2	–	−89	–	dBm
	MCS 1	–	−91	–	dBm
	MCS 0	–	−94	–	dBm
	40 MHz channel spacing for all MCS rates				
	MCS 15	–	−67	–	dBm
	MCS 8	–	−86	–	dBm
	MCS 7	–	−71	–	dBm
	MCS 6	–	−73	–	dBm
	MCS 5	–	−75	–	dBm
	MCS 4	–	−79	–	dBm
	MCS 3	–	−82	–	dBm
	MCS 2	–	−86	–	dBm
	MCS 1	–	−88	–	dBm
	MCS 0	–	−90	–	dBm

Table 11: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
IEEE 802.11ac RX sensitivity (10% PER for 4096 octet PSDU)[a] Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS 8	−59	−70	–	dBm
	MCS 7	−64	−74	–	dBm
	MCS 6	−65	−75	–	dBm
	MCS 5	−66	−74	–	dBm
	MCS 4	−70	−81	–	dBm
	MCS 3	−74	−84	–	dBm
	MCS 2	−77	−87	–	dBm
	MCS 1	−79	−90	–	dBm
	MCS 0	−82	−93	–	dBm
	40 MHz channel spacing for all MCS rates				
	MCS 9	−54	−66	–	dBm
	MCS 8	−56	−67	–	dBm
	MCS 7	−61	−73	–	dBm
	MCS 6	−62	−72	–	dBm
	MCS 5	−63	−72	–	dBm
	MCS 4	−67	−79	–	dBm
	MCS 3	−71	−82	–	dBm
	MCS 2	−74	−85	–	dBm
	MCS 1	−76	−87	–	dBm
	MCS 0	−79	−90	–	dBm
	80 MHz channel spacing for all MCS rates				
	MCS 9	−51	−62	–	dBm
	MCS 8	−53	−64	–	dBm
	MCS 7	−58	−68	–	dBm
	MCS 6	−59	−68	–	dBm
	MCS 5	−60	−73	–	dBm
	MCS 4	−64	−75	–	dBm
	MCS 3	−68	−78	–	dBm
	MCS 2	−71	−81	–	dBm
	MCS 1	−73	−83	–	dBm
	MCS 0	−76	−87	–	dBm
Input In-Band IP3[a]	Maximum LNA gain	–	−15.5	–	dBm
	Minimum LNA gain	–	−1.5	–	dBm
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mbps	−9.5	–	–	dBm
	@ 18, 24, 36, 48, 54 Mbps	−14.5	–	–	dBm
LPF 3 dB bandwidth	–	−9	–	36	MHz

Table 11: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[b] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–78.5 dBm	32	–	–	dB
	9 Mbps OFDM	–77.5 dBm	31	–	–	dB
	12 Mbps OFDM	–75.5 dBm	29	–	–	dB
	18 Mbps OFDM	–73.5 dBm	27	–	–	dB
	24 Mbps OFDM	–70.5 dBm	24	–	–	dB
	36 Mbps OFDM	–66.5 dBm	20	–	–	dB
	48 Mbps OFDM	–62.5 dBm	16	–	–	dB
	54 Mbps OFDM	–61.5 dBm	15	–	–	dB
IEEE 802.11ac adjacent channel rejection MCS0–9 (Difference between interfering and desired signal at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/ Notes)	MCS9	–57 dBm	–9	–	–	dB
	MCS8	–59 dBm	–7	–	–	dB
	MCS7	–64 dBm	–2	–	–	dB
	MCS6	–65 dBm	–1	–	–	dB
	MCS5	–66 dBm	0	–	–	dB
	MCS4	–70 dBm	4	–	–	dB
	MCS3	–74 dBm	8	–	–	dB
	MCS2	–77 dBm	11	–	–	dB
	MCS1	–79 dBm	13	–	–	dB
	MCS0	–82 dBm	16	–	–	dB
Maximum receiver gain	–		95	–	–	dB
Gain control step	–		3	–	–	dB
RSSI accuracy[c]	Range –98 dBm to –30 dBm		–5	–	5	dB
	Range above –30 dBm		–8	–	8	dB
Return loss	Z_o = 50Ω		–10	–	13	dB
Receiver cascaded noise figure	At maximum gain		–	4	–	dB

a. Derate by 1.5 dB for –30 °C to –10°C and 55°C to 85°C.
b. For 65 Mbps, the size is 4096.
c. The minimum and maximum values shown have a 95% confidence level.

WLAN 5 GHz Transmitter Performance Specifications

Note: The specifications in Table 12 are measured at the chip port, unless otherwise specified.

Table 12: WLAN 5 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		4900	–	5845	MHz
Harmonic level (at –5 dBm)	9.8–11.570 GHz	2nd harmonic	–	–31	–	dBm/MHz
Tx power at RF port for highest power level setting at 25°C and VBAT = 3.6V with spectral mask and EVM compliance[a, b]	OFDM, QPSK	–13 dB	4	5	–	dBm
	OFDM, 16-QAM	–19 dB	2.5	4	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	1.5	3	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	0.5	2	–	dBm
	OFDM, 256-QAM (R = 3/4, VHT20)	–30 dB	TBD	–	–	dBm
	OFDM, 256-QAM (R = 5/6, VHT20)	–32 dB	TBD	–	–	dBm
Phase noise	37.4 MHz crystal, Integrated from 10 kHz to 10 MHz		–	0.5	–	Degrees
Tx power control dynamic range	–		10	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Z_o = 50Ω		–	6	–	dB

a. Derate by 1.5 dB for temperatures less than –10°C or more than 55°C, or voltages less than 3.0V. Derate by 3.0 dB for voltages of less than 2.7V, or voltages of less than 3.0V at temperatures less than –10°C or greater than 55°C. Derate by 4.5 dB for –40°C to –30°C.

b. Tx power for Channel 1 and Channel 11 is specified by non-volatile memory parameters.

General Spurious Emissions Specifications

Table 13: General Spurious Emissions Specifications[a]

Parameter	*Condition/Notes*		*Min*	*Typ*	*Max*	*Unit*
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
Tx Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–93	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–45.5	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–72	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–87	–	dBm
Rx/standby Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–107	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–65a	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–87	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–100	–	dBm

a. For frequencies other than 3.2 GHz, the emissions vale is –96 dBm. The value in the table is the result of LO leakage at 3.2 GHz.

Section 7: Timing Characteristics

Power Sequence Timing

The recommended power-up sequence is to bring up the power supplies in the order of the rated voltage. This means that the 3.3V power supply should be powered up first, followed by the 1.2V supply. The recommended power-up sequence, which is illustrated in Figure 9, minimizes the possibility of a latch-up condition. The power-up timing parameters are shown in Table 14.

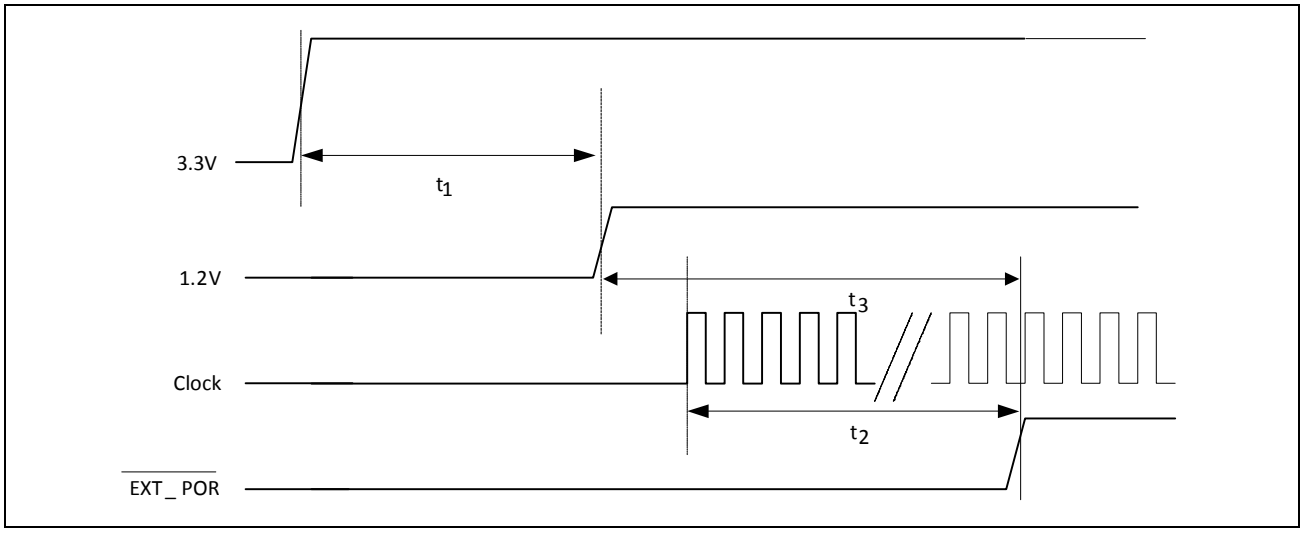


Figure 9: Power-Up Sequence Timing Diagram

Table 14: Power-Up Timing Parameters

Symbol	*Description*	*Minimum*	*Typical*	*Maximum*	*Unit*
t_1	3.3V active to 1.2V active	1	–	3.2	ms
t_2	Clock stable to reset deasserted	5	–	–	ms
t_3	1.2V active to reset deasserted	–	40	–	ms

SPROM Timing Diagram

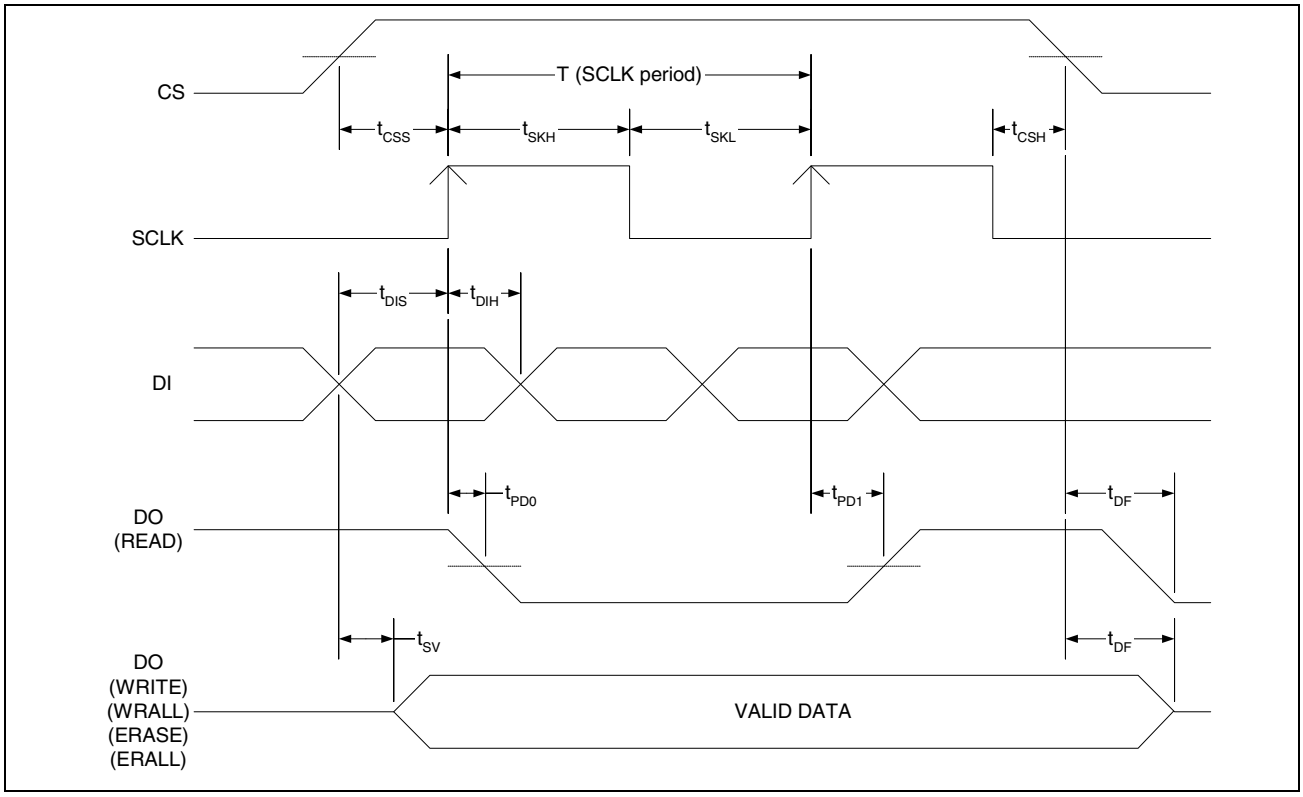


Figure 10: SPROM Timing Diagram

Table 15: SPROM Timing

Timing Symbol	*Parameter*	*Minimum*	*Maximum*	*Units*
f_{SK}	SCLK Clock Frequency	0	1	MHz
t_{SKH}	SCLK High Time	250	–	ns
t_{SKL}	SCLK Low Time	250	–	ns
t_{CS}	Minimum CS Low Time	250	–	ns
t_{CSS}	CS Setup Time	50	–	ns
t_{DIS}	DI Setup Time	100	–	ns
t_{CSH}	CS Hold Time	0	–	ns
t_{DIH}	DI Hold Time	100	–	ns
t_{PD0}	Output Delay to 1	–	500	ns
t_{PD1}	Output Delay to 0	–	500	ns
t_{SV}	CS to Data Valid	–	500	ns
t_{DF}	CS to DO in 3-state	–	100	ns
t_{WP}	Write Cycle Time	–	10	ms

Section 8: Thermal Information

JDEC Thermal Characteristics

Table 16: JEDEC Thermal Characteristics, 12 × 12 Package [a]

Power Dissipation (W)	2.47				
Ambient Air Temperature (°C)	70				
θ_{JB} (°C/W)	0.88				
θ_{JC} (°C/W)	8.34				
Airflow	0 fpm, 0 mps	100 fpm, 0.508 mps	200 fpm, 1.016 mps	400 fpm, 2.032 mps	600 fpm, 3.048 mps
T_J (°C)	117.5	111.6	109.0	106.3	104.9
θ_{JA} (°C/W)	19.22	16.86	15.80	14.71	14.11
Ψ_{JT} (°C/W)	0.41	0.44	0.55	0.59	0.60

a. No heat sink, TA = 70°C. This is an estimate based on 4-layer 2s2p PCB and P = 2.47W.

Note:

- Ambient air temperature: TA = 55°C.
- The BCM43526 is designed and rated for operation at a maximum junction temperature not to exceed 125°C.

Junction Temperature Estimation and PSI_{JT} Versus $Theta_{JC}$

Package thermal characterization parameter Psi-J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is as follows:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

- T_J = junction temperature at steady-state condition, °C
- T_T = package case top center temperature at steady-state condition, °C
- P = device power dissipation, Watts
- Ψ_{JT} = package thermal characteristics (no airflow), °C/W

Ordering Information

Table 17: Ordering Information

Part Number	*Package*	*Ambient Temperature*
BCM43526KMLG	12 × 12, 108-pin QFN (RoHs compliant)	0° C to 70° C (32° F to 158° F)

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